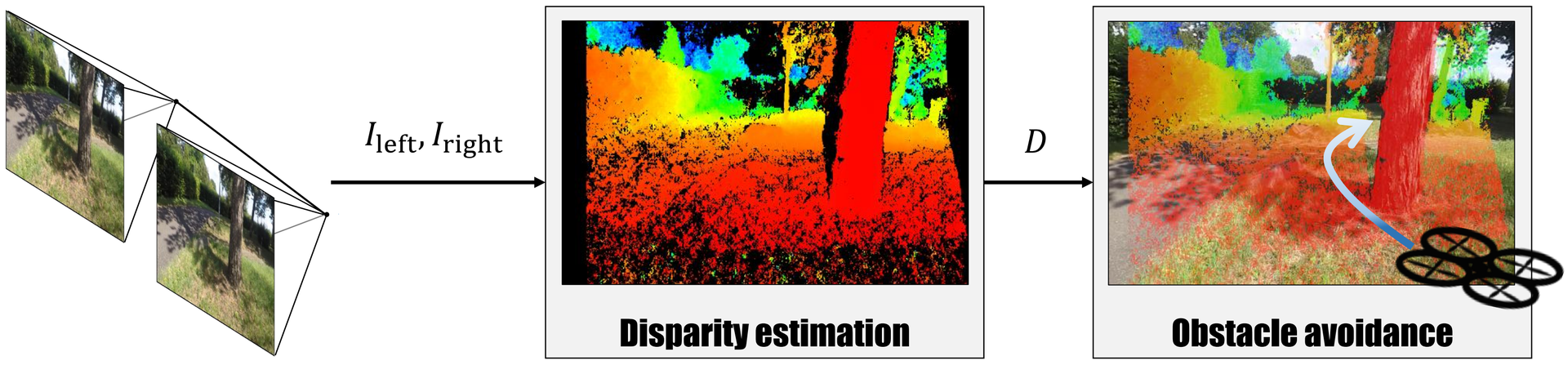
Towards Ubiquitous Low-power Image Processing Platforms

Horizon 2020

The UAV Use-case: real-time obstacle avoidance for UAVs



The Algorithm

Disparity Estimation

- Stereo disparity estimation based on SGM, directly synthesized form C/C++ with HLS and deployed on embedded FPGA
  1. Image rectification and matching
  2. 4-path SGM optimization, adopted for streamed processing
  3. Left-Right check and Median filtering

Obstacle Avoidance

- Reactive obstacle avoidance algorithm computing shortest path around obstacle based on disparity map
  1. U- / V-Map computation
  2. Binary filtering and contour detection
  3. Obstacle extraction and waypoint computation

The Implementation

Runtime measurements

Operation	Time [ms]	Avg. Time [ms]
Disparity Estim. (FPGA)	31.4 – 36.1	34.5
Obstacle Avoid. (CPU)	2.7 – 11.0	4.2
Total	34.1 – 47.1	38.7

Disparity estimation deployed on FPGA running at 200 MHz

- Up to 29 Hz and a latency of 28.5 ms at a frame size of 640x360 pixel and 60 disparities

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