TECHNISCHE UNIVERSITÄT DRESDEN

Faculty of Computer Science, Institute of Computer Engineering, Chair of Adaptive Dynamic Systems

Low Power Image Processing Applications on FPGAs using Dynamic Voltage Scaling and Partial Reconfiguration

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Abstract

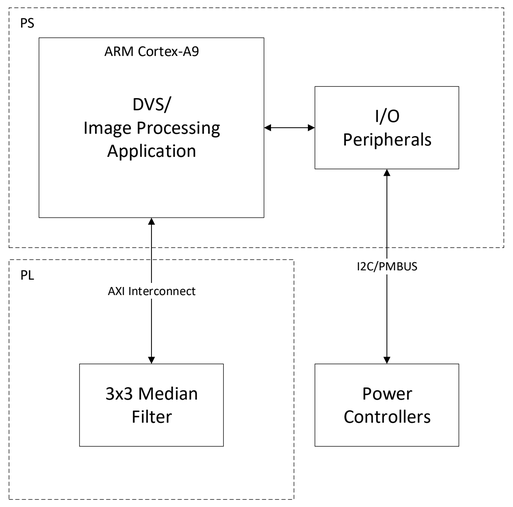
The TULIPP project aims to facilitate the development of embedded image processing systems with real-time and low-power constraints. In this work, several adaptive dynamic run-time techniques for reconfigurable SoCs are described. These methods are used for low power image processing applications on high-performance embedded platforms. Dynamic Voltage Scaling (DVS) and Dynamic Partial Reconfiguration (DPR) target the low-power requirements of the embedded systems while debugging supports the fast development on the hardware side of the system. The proposed techniques were tested and verified using an own developed custom SDSoC image processing library.

Overview

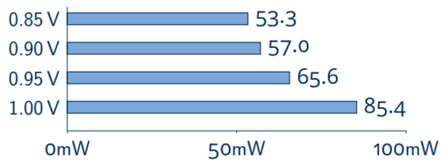
- **Low power image processing applications on the EMC²-TULIPP platform.**
- **Meeting the Real-time requirements through FreeRTOS.**
- **Implementation of a parameterizable andstreaming based High-Level Synthesis image processing library.**
- **Reduction of power consumption through the run-time techniques Dynamic Partial Reconfiguration and Dynamic Voltage Scaling.**
- **More visibility through self-developed Debugging system.**

Dynamic Voltage Scaling

- **Used for power management at run-time.**
- **Power optimization through Dynamic Voltage Scaling (DVS) application running on Processing System (PS).**



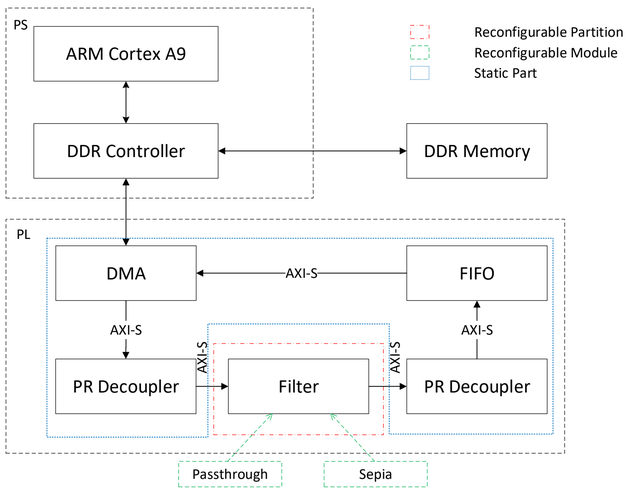
- **Power reduction of Programmable Logic (PL) by 37.6%.**



Resource	Used	Total	% Utilization
BRAM	18	140	12.9
LUT	9842	53200	18.5
FF	11984	105400	11.3

Dynamic Partial Reconfiguration

- **Used to change the functionality of a selected area**
- **Control the Dynamic Partial Reconfiguration process from the Processing System (PS).**

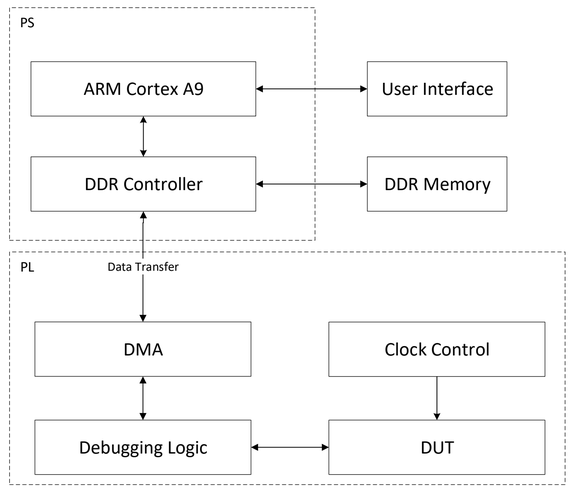


- **Main features of Dynamic Partial Reconfiguration:**
  - **– Reduction of power consumption**
  - **– Increase hardware resources sharing.**
  - **– Change the filter behaviour without halting the complete system.**

Parameter	Value
Partial Bitstream Size	1250 Kbytes
Reconfiguration Time	10 ms

Debugging System

- **Hardware suffers from inherent invisibility.**
- **Provision of full visibility through effectively unlimited debug window.**



- **Main features of the debugging system:**
  - **– Resource efficient debugging with multiple options of trace window.**
  - **– Lossless debugging regardless of the trace window.**

Window	Resource	Used	Total	% Utilization
64	BRAM	9	265	3.4
64	LUT	2617	78600	3.3
64	FF	3757	157200	2.4
1024	BRAM	18	265	6.8
1024	LUT	3136	78600	4
1024	FF	4134	157200	2.6

Further Information

Ariel Podlubne, Julian Haase, Lester Kalms, Gökhan Akgün, Muhammad Ali, Habib ul hasan Khan, Ahmed Kamal and Diana Göhringer. "Low Power Image Processing Applications on FPGAs using Dynamic Voltage Scaling and Partial Reconfiguration". 2018 Conference on Design and Architectures for Signal and Image Processing (DASIP), Porto, 2018

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