Power Profiling Of Embedded Vision Applications In The TULIPP Project

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ABSTRACT

The TULIPP project aims to demonstrate guidelines that simplify development of embedded vision applications with low-power and real-time requirements. Guidelines related to low-power execution and energy savings have proven difficult to demonstrate since the high-performance embedded platform chosen by the project has poor power profiling support. This limitation plagues most embedded platforms in general and practitioners have adopted ad-hoc methods to cope. In this short paper, we report our on-going effort to advance the state-of-the-art in power profiling of embedded vision applications through low-cost measurement hardware and specialized profiling tools. The desired end result is to enable power measurements that can be correlated with application execution at varying levels of detail.

CCS CONCEPTS

• **Computer systems organization → Embedded hardware**; **Real-time operating systems**; • **Hardware → Platform power issues**;

KEYWORDS

Profiling; Low-power; Performance Analysis; Embedded Vision; Image Processing

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1 INTRODUCTION

The TULIPP project deals with applications from Unmanned Aerial Vehicles (UAV), Surgical Equipment, and Advanced Driver Assistance Systems (ADAS) domains [15]. These applications pose low-power execution as a first-class requirement since a good low-power design simplifies heat dissipation systems, lowers weight, and runs longer per battery-charge cycle without sacrificing performance.

Improving the power efficiency of embedded applications begins with prudent device selection. For example, choosing FPGAs made with latest FinFET technology [1]. Once the device is fixed, power efficiency is refined to desired levels in successive stages of profiling and optimization. Profiling uses power models during early design phases, and shifts to real-hardware measurements post-implementation. While standard power profiling methods are available for HPC-like systems [9], power profiling in embedded systems remains largely ad-hoc [2, 4, 7, 10, 18].

The Xilinx Zynq-based [21] embedded platform chosen for applications of the TULIPP project has poor support for power profiling. Neither hardware nor vendor tools have support for measuring power consumption at runtime. This complicates selection of application phases to direct power optimizations and makes it difficult to judge whether low-power requirements are met. Ultimately, a key contribution of the project – guidelines for low-power embedded vision – cannot be demonstrated.

To solve this problem, we first looked towards solutions recommended by vendors. Xilinx recommends adding on-board current sensors such as precision shunt resistors to provide current measurements to the XADC [20], a hard-IP block in the FPGA substrate of the Zynq. A better solution, also recommended by Xilinx, is to replace the voltage regulators on the hardware platform with digital power controllers from Texas Instruments (TI) to measure current and voltages supplied to all power planes [16]. Another option is to use special measurement-friendly variants of the embedded platform built by third-parties [12]. While useful, these recommended hardware modifications were prohibitive due to cost reasons.

We also deliberated about a model-only approach i.e., use the Xilinx-provided power model called the *XPE* [18] to refine power efficiency as much as possible during early design phases. However, XPE can at best provide coarse-grained estimates and cannot correlate power problems with application phases.

We decided in the end to build external, cost-effective measurement hardware, complemented by specialized profiling software, to diagnose power problems of TULIPP applications at runtime and in general, advance the state-of-the-art in power profiling of embedded vision applications. In this short paper, we report on-going effort towards our goal. The desired end result is to enable power measurements that can be correlated with application execution at varying levels of detail. The detail levels include hardware units such as memory subsystems, processors, and FPGA-blocks, and software units such as communication events, compiler-generated intermediate representations, and functions in source code.

2 THE TULIPP PROJECT

We describe the TULIPP project in brief in this section.

The foremost planned contribution of TULIPP is a *Starter Kit* that simplifies development of embedded vision applications [15]. The audience for the Starter Kit includes both novice engineers and image processing experts. The development of the Starter Kit and its eventual entry into influential ecosystems is scrutinized by an advisory board consisting of experts from industry and academia.

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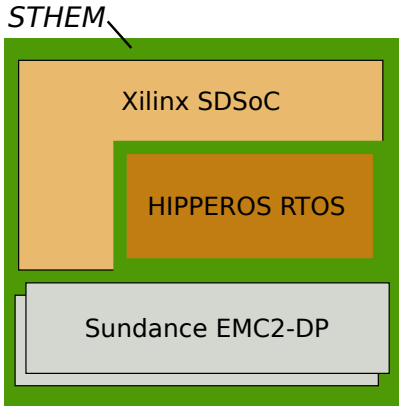

Figure 1: The TULIPP-PI1 platform with STHEM adaptations

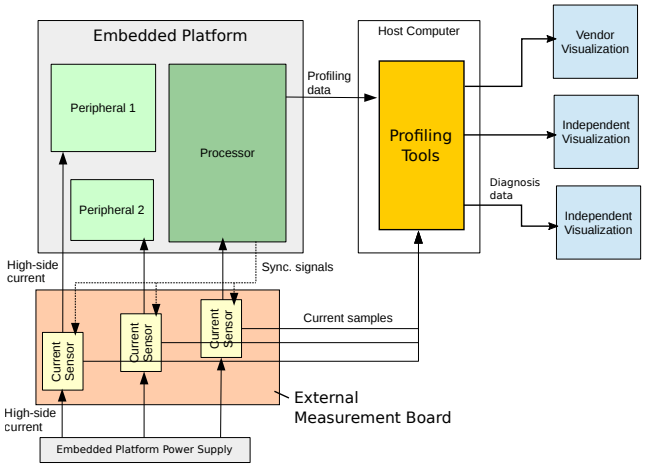

Figure 2: Overview of power profiling

The central component of the Starter Kit is a set of guidelines that recommends productive implementation methods, provides concrete advice on problem solving, and weighs tradeoffs. The guidelines are validated and exemplified in relevant applications from UAV, Surgical Equipment, and ADAS domains. These demonstrator applications have real-time, low-power requirements and are built for a high-performance embedded platform called the *TULIPP-PI1*.

The TULIPP-PI1 is a custom platform conceived by the industrial partners of the project. It consists of the EMC2-DP carrier board by Sundance arranged in a stacked, two-board configuration [14]. Each EMC2-DP houses the Xilinx Zynq 7000 SoC-FPGA [21] as a System-on-Module (SoM). The two-board hardware is operated seamlessly by the HIPPEROS RTOS [13]. Application development tools in TULIPP-PI1 include SDSoC from Xilinx [19] and build tools from HIPPEROS.

Custom adaptations, collectively called *STHEM*, are made to all TULIPP-PI1 components to support two-board hardware acceleration, real-time constraints, and low-power execution. STHEM includes interfacing tools that glue together incompatible-by-default vendor components together and standalone tools that extend existing functionality to provide complementary features. An illustration of TULIPP-PI1 with STHEM is shown in Figure 1. The power profiling infrastructure discussed in the paper is a part of STHEM.

3 POWER PROFILING

Our power profiling approach essentially consists of an external measurement board that communicates power measurements to profiling tools on the host computer, as shown in Figure 2. The external measurement board is custom-designed and has multiple current sensors that measure power consumed by individual *units of interest* on the embedded platform i.e., the EMC2-DP board in TULIPP-PI1. Profiling tools collect additional profiling data from EMC2-DP and analyze it together with power measurements to diagnose problems. Problems are shown on various visualization widgets, some of which are part of existing vendor tools.

3.1 Lynsyn

We refer to the first version of the external measurement board as *Lynsyn*. Lynsyn uses two INA169 current-shunt monitors [6] from TI to measure and amplify currents across 0.1 Ohm shunt resistors connected in series with high-side current wires/PCB-tracks that drive units of interest on the EMC2-DP. Measurements from the current-shunt monitors are sampled by a Teensy 3.6 microcontroller [11] using 13-bits and transmitted over USB to the host computer at approximately 12K samples per second. This rate supports application tasks up to 83 micro seconds. Synchronization signals are sent over JTAG and LVTTL GPIO ports on the EMC2-DP to the Teensy to control measurements. At present, we consider two units of interest – the Zynq SoM and the FMC port that connects to the camera. Lynsyn can sense currents between 250 mA to 3 A. Measuring currents lower than 250 mA is possible by using larger shunt resistors. The BOM cost of Lynsyn is less than 50 US dollars.

We validated current measurements from Lynsyn using the Uni-T UT139C true-RMS digital multimeter for two hours of continuous operation. Current measurements had negligible differences compared to the UT139C. More rigorous testing with a constant current load is planned as part of future work.

Lynsyn's design assumes that it is possible to insert shunt resistors in all current-carrying lines of interest. However, not all current-carrying lines are accessible. For example, rails that supply power to the FPGA substrate of the Zynq SoM are buried due to dense packaging constraints. Potential workarounds include using current-mirrors to avoid inserting shunt resistors [7], or using special test fixtures that expose current-carrying lines on top layers [12].

A protoboard version of Lynsyn connected to the EMC2-DP (non-stacked) is shown in Figure 3.

3.2 Visualizations

Current samples sent from Lynsyn to the host computer are converted to power readings assuming a constant supply voltage and stored in the Common Trace Format (CTF) [5] by a profiling tool.

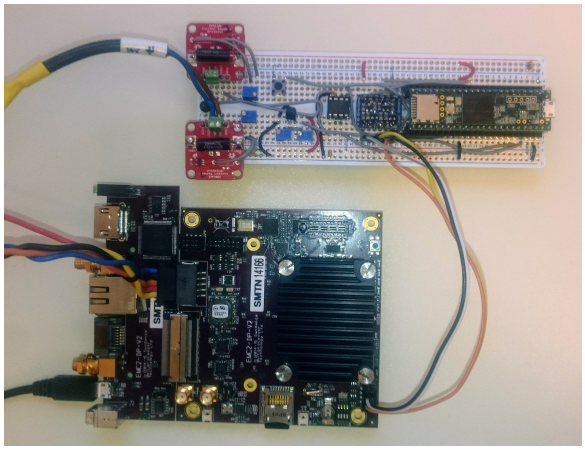

Figure 3: Lynsyn, the power measurement board (top) connected the EMC2-DP. The thick wire connects to a current sensor. The thin wires carry synchronization signals.

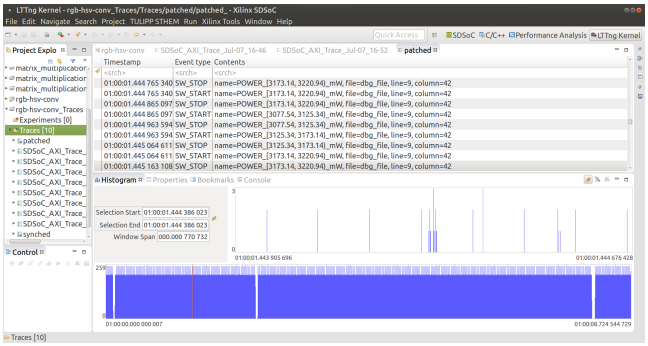

Figure 4: Inspecting a power trace on Trace Compass

CTF is a flexible, high-throughput, binary trace format developed by the Multicore Association.

The power traces can be visualized using Trace Compass, an open-source, standalone viewer popularized by the Linux Tracing Toolkit (LTTng) project [3]. Trace Compass enables correlation and filtering of power traces. An example is provided in Figure 4.

We visualize instantaneous power computed from the current samples on a running line graph as shown in Figure 5. This helps understand power trends at real-time as the application executes. Abrupt, large changes in power values are flagged on the visualization to alert users.

SDSoC enables users to understand timing of application events in a timeline visualization called the *AXI Trace Viewer* [17]. We extend the AXI Trace Viewer to visualize power traces correlated with application phases. This enables programmers to conveniently attribute power consumption to concurrent application events and isolate power problems. However, we are not able to refine user interaction in this mode since SDSoC is closed-source software.

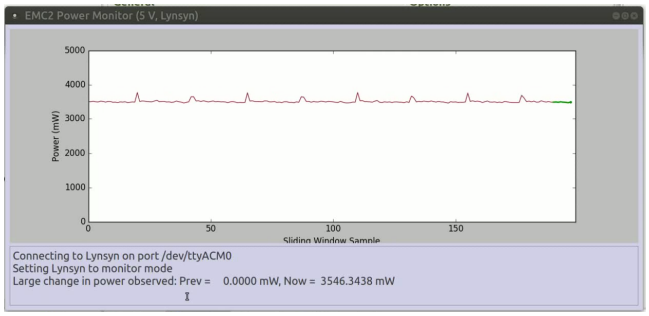

Figure 5: Power monitor visualization tracks instantaneous power consumption during application execution

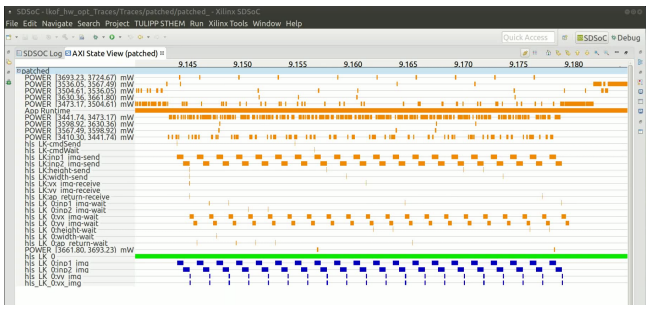

Figure 6: Attributing power consumption to application events on SDSoC's AXI Trace Viewer

4 CONCLUSION AND FUTURE WORK

We presented on-going effort towards building power profiling infrastructure for embedded vision applications in the TULIPP project. Our current approach is to use external, cost-effective, custom-built measurement hardware, complemented by specialized profiling software, to diagnose power problems at runtime. As part of future work, we intend to profile application-specific data such as the program counter and parallelization events while collecting power samples. The idea is to analyze this data to pinpoint power problems on high-level semantic visualizations such as basic-block graphs (Figure 7) and grain graphs (Figure 8) [8].

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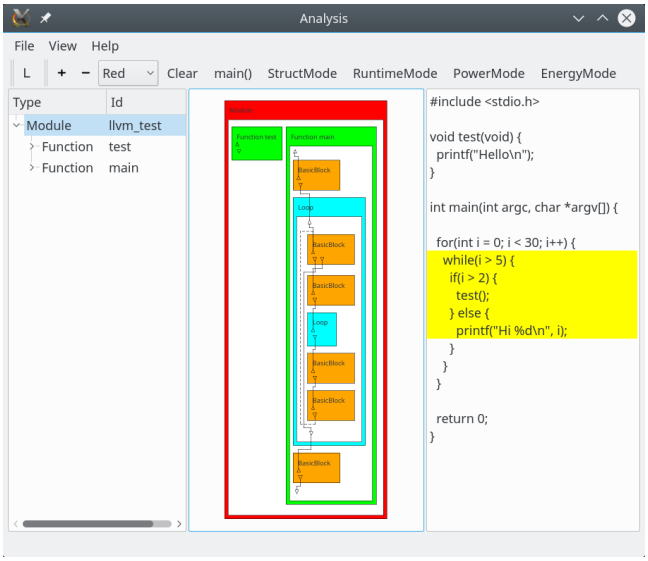

Figure 7: Visualizing compiler-generated intermediate representation as a precursor to diagnosing power problems

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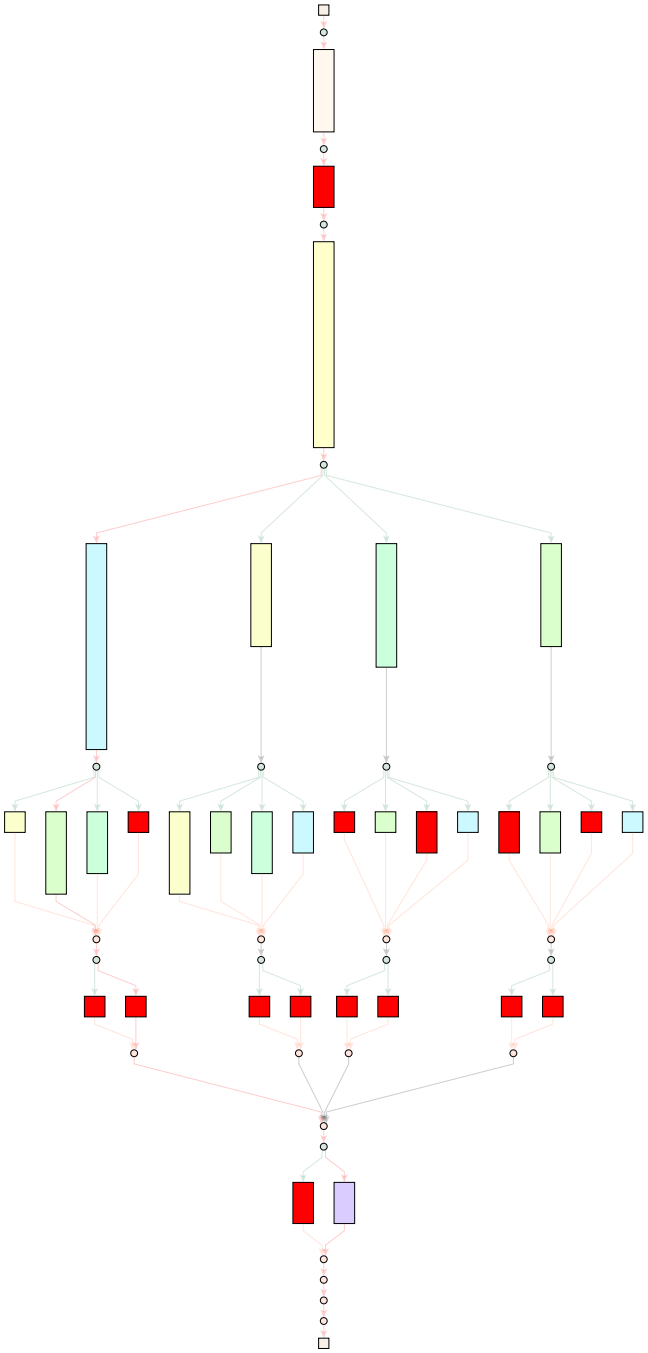

Figure 8: Visualizing grain graphs (OpenMP) as a precursor to diagnosing power problems